		-1 - Do	Docket No. 0819-0653				
IN THE UNITED STA	ATES	PATENT AND TRADEMARK OF	FICE RECEIVED				
Te In of Patent Application of	)	E. Willis 8-27-02	FEB 13 2002				
Keiichi FUJIMOTO et al	)	Attention: Applications Branch	TC 2800 MAIL ROOM				
Serial No. 09/964,480	)	I hereby certify that this correspondence is being deposited with The United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on December 20,2001					
Filed: September 28, 2001	)						
For: SEMICONDUCTOR	)						
INTEGRATED CIRCUIT	)						
TESTING SYSTEM AND	)						
METHOD	)	Attention: Application Processing	ng Division				

## REQUEST FOR CORRECTED FILING RECEIPT

Honorable Commissioner of Patents

Washington, D.C. 20231

Sir:

The Filing Receipt received in the above-identified application has errors thereon due to Patent Office error as shown in red on the attached copy.

In view of the above, it is requested that a Corrected Filing Receipt be issued.

Respectfully submitted,

Eric J. Robinson

Registration No. 38,285

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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS	ĺ
09/964,480	09/28/2001	2858	710	740819-653	9	12	2	

**CONFIRMATION NO. 2785** 

22204 NIXON PEABODY, LLP 8180 GREENSBORO DRIVE SUITE 800

MCLEAN, VA 22102

FILING RECEIPT

\*OC0000000006954805\*

Date Mailed: 10/30/2001

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Keiichi Fujimoto, Kyoto, JAPAN; Yoshiro Nakata, Ocaka, JAPAN; Kyoto

Domestic Priority data as claimed by applicant

**Foreign Applications** 

JAPAN 2001-028597 02/05/2001

If Required, Foreign Filing License Granted 10/23/2001

Projected Publication Date: 08/08/2002

Non-Publication Request: No

Early Publication Request: No

NOV 0 1 2001

2800 MAIL ROOM

**Title** 

Semiconductor integrated circuit testing system and method

**Preliminary Class** 

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